

WHAT IS CLAIMED IS:

1. A superscalar processor for performing out of order processing on an instruction set having a plurality of instructions and a plurality of architectural registers associated therewith, the superscalar processor comprising:
  - at least one execution unit for executing a plurality of in-flight instructions of the instruction set;
  - a plurality of physical registers;
  - a fetch unit for fetching the instructions from the instruction set;
  - an instruction renaming unit (IRU) for renaming architectural registers to physical registers during the processing of the instruction set;
  - an instruction scheduling unit (ISU) for scheduling the in-flight instructions for execution, the ISU including a dependency matrix for storing dependency data of the in-flight instructions and an instruction wait buffer (IWB) for storing physical register address data necessary to execute the in-flight instructions when the dependency matrix indicates that the dependencies of the in-flight instructions have been removed; and
  - a content addressable memory (CAM) structure having a comparator section mapped to an array section, the CAM structure transmitting a first output signal for generating the dependency data stored in the dependency matrix and a second output signal for generating the physical register address data stored in the IWB.
2. The superscalar processor of Claim 1 wherein the CAM structure further comprises a plurality of CAM structures each having a first and second output signal, the first output signals being logically OR-ed together at an ORing unit to generate the dependency data.

3. The superscalar processor of Claim 2 wherein the instructions have a first predetermined maximum number of register source fields (RS fields) and at least a maximum number of one register destination fields (RD fields), and wherein the CAM structures further comprise the first predetermined maximum number of CAM structures, each CAM structure being dedicated to a single RS field.

4. The superscalar processor of Claim 1 wherein the instructions have a first predetermined maximum number of register source fields (RS fields) having architectural addresses for instruction input data and at least a maximum number of one register destination fields (RD fields) having architectural addresses for instruction output data, and wherein the CAM structure further comprises:

the comparator section including a register dependency checker (RDC) for comparing an RS field of a fetched instruction to an RD field of an in-flight instruction; and

the first output signal including a hit detect signal indicative of the architectural address of the RD field which is generated when a match, i. e., hit, between the RS field and the RD field is detected by the RDC, the hit detect signal additionally being transmitted to the array section of the CAM structure .

5. The superscalar processor of Claim 4 wherein the CAM structure further comprises:

the array section including an in-flight physical register mapper (IPM); and

the second output signal including an output signal of the IPM indicative of the physical register address of the RD field which is generated when the IPM receives the hit detect signal.

6. The superscalar processor of Claim 4 wherein the CAM structure further comprises a plurality of the first predetermined number of CAM structures, each CAM structure being dedicated to a single RS field.

7. The superscalar processor of Claim 6 wherein the hit detect signals of each CAM structure are logically OR-ed together at an ORing unit to generate the dependency data.

8. The superscalar processor of Claim 7 further comprising:  
the plurality of physical registers including a queue area for storing a second predetermined maximum number of in-flight instructions of the instruction set; and

5 the fetch unit fetching a bundle having a third predetermined fixed number of instructions from the instruction set.

9. The superscalar processor of Claim 8 further comprising an intra dependency checker having an output signal indicative of the dependencies between the instructions in the bundle, the output signal of the intra dependency checker being combined with the OR-ed output signals of the hit  
5 detect signals to generate the dependency data.

10. The superscalar processor of Claim 9 wherein the RDC further comprises:  
a plurality of the second predetermined number of entry structures, each entry structure including a plurality of the third predetermined number of comparators, each comparator dedicated to a single instruction in the bundle;  
5 wherein

each RD field of the in-flight instructions is compared by a single entry structure to all instructions in the bundle substantially simultaneously.

11. The superscalar processor of Claim 10 wherein the hit detect signal further comprises an array of the second predetermined number by the third predetermined number in size, which includes the output of hits detected for each of the entry structures compared to each of the instructions in the bundle.

12. A superscalar processor for performing out of order processing on an instruction set having a plurality of instructions and a plurality of architectural registers associated therewith, which have a first predetermined maximum  
 5 number of register source fields (RS fields) and at least a maximum number of one register destination field (RD field), the superscalar processor comprising:  
     at least one execution unit for executing a plurality of in-flight instructions of the instruction set;  
     a plurality of physical registers;  
 10     a fetch unit for fetching the instructions from the instruction set;  
     an instruction renaming unit (IRU) for renaming architectural registers to physical registers during the processing of the instruction set;  
     an instruction scheduling unit (ISU) for scheduling the in-flight instructions for execution, the ISU including a dependency matrix for storing  
 15 dependency data of the in-flight instructions and an instruction wait buffer (IWB) for storing physical register address data necessary to execute the in-flight instructions when the dependency matrix indicates that the dependencies of the in-flight instructions have been removed; and  
     a first predetermined number of content addressable memory (CAM)  
 20 structures having a comparator section mapped to an array section, each CAM structure being dedicated to a single RS field and transmitting a first and second output signal, the first output signals of each CAM structure being logically OR-ed together at an ORing unit for generating the dependency data stored in the dependency matrix and the second output signals for each CAM structure being  
 25 combined together for generating the physical register address data stored in the IWB.

13. The superscalar processor of Claim 12 wherein the RS fields have architectural addresses for instruction input data and the RD fields have architectural addresses for instruction output data, and wherein the CAM structures further comprise:

5 the comparator sections including a register dependency checker (RDC) for comparing an RS field of a fetched instruction to an RD field of an in-flight instruction;

the first output signals including a hit detect signal indicative of the architectural address of the RD field which is generated when a match, i. e., hit,  
10 between the RS field and the RD field is detected by the RDC, the hit detect signal additionally being transmitted to the array sections of the CAM structures;

the array sections including an in-flight physical register mapper (IPM);  
and

15 the second output signals including an output of the IPM indicative of the physical register address of the RD field which is generated when the IPM receives the hit detect signal.

14. The superscalar processor of Claim 13 further comprising:

the plurality of physical registers including a queue area for storing a second predetermined maximum number of in-flight instructions of the instruction set;

5 the fetch unit fetching a bundle having a third predetermined number of instructions from the instruction set; and

the RDC further including a plurality of the second predetermined number of entry structures, each entry structure including a plurality of the third predetermined number of comparators, each comparator dedicated to a  
10 single instruction in the bundle;  
wherein each RD field of the in-flight instructions is compared by a single entry structure to all instructions in the bundle substantially simultaneously to generate the hit detect signal.

15. A computer system comprising:

a bus;

an input/output subsystem for interfacing with input/output devices;

a memory subsystem having a memory for storing an instruction set

5 having a plurality of instructions and a plurality of architectural registers associated therewith; and

a superscalar processor for performing out of order processing on the instruction set and being in communication with the input/output subsystem and the memory subsystem through the bus, the superscalar processor

10 including,

at least one execution unit for executing a plurality of in-flight instructions of the instruction set,

a plurality of physical registers,

a fetch unit for fetching the instructions from the instruction set,

15 an instruction renaming unit (IRU) for renaming architectural registers to physical registers during the processing of the instruction set,

an instruction scheduling unit (ISU) for scheduling the in-flight instructions for execution, the ISU including a dependency matrix for storing dependency data of the in-flight instructions and an instruction wait buffer (IWB) for storing physical register address data necessary to execute the in-flight instructions when the dependency matrix indicates that the dependencies of the in-flight instructions have been removed, and

20 a content addressable memory (CAM) structure having a comparator section mapped to an array section, the CAM structure transmitting a first output signal for generating the dependency data stored in the dependency matrix and a second output signal for generating the physical register address data stored in the IWB.

16. The computer system of Claim 15 wherein the CAM structure further comprises a plurality of CAM structures each having a first and second output signal, the first output signals being logically OR-ed together at an ORing unit to generate the dependency data.

5

17. The computer system of Claim 16 wherein the instructions have a first predetermined maximum number of register source fields (RS fields) and at least a maximum number of one register destination fields (RD fields), and wherein the CAM structures further comprise the first predetermined maximum  
5 number of CAM structures, each CAM structure being dedicated to a single RS field.

18. The computer system of Claim 15 wherein the instructions have a first predetermined maximum number of register source fields (RS fields) having an architectural addresses for instruction input data and at least a maximum number of one register destination fields (RD fields) having architectural  
5 addresses for instruction output data, and wherein the CAM structure further comprises:

the comparator section including a register dependency checker (RDC) for comparing an RS field of a fetched instruction to an RD field of an in-flight instruction; and

10 the first output signal including a hit detect signal indicative of the architectural address of the RD field which is generated when a match, i. e., hit, between the RS field and the RD field is detected by the RDC, the hit detect signal additionally being transmitted to the array section of the CAM structure.

19. The computer system of Claim 18 wherein the CAM structure further comprises:

the array section including an in-flight physical register mapper (IPM);  
and

5 the second output signal including an output signal of the IPM indicative of the physical register address of the RD field which is generated when the IPM receives the hit detect signal.

20. The computer system of Claim 18 wherein the CAM structure further comprises a plurality of the first predetermined number of CAM structures, each CAM structure being dedicated to a single RS field.

21. The computer system of Claim 20 wherein the hit detect signals of each CAM structure are logically OR-ed together at an ORing unit to generate the dependency data.

22. The computer system of Claim 21 further comprising:

the plurality of physical registers including a queue area for storing a second predetermined maximum number of in-flight instructions of the instruction set; and

5 the fetch unit fetching a bundle having a third predetermined fixed number of instructions from the instruction set.

23. The computer system of Claim 22 further comprising an intra dependency checker having an output signal indicative of the dependencies between the instructions in the bundle, the output signal of the intra dependency checker being combined with the OR-ed output signals of the hit  
5 detect signals to generate the dependency data.



24. The computer system of Claim 23 wherein the RDC further comprises:  
a plurality of the second predetermined number of entry structures, each  
entry structure including a plurality of the third predetermined number of  
comparators, each comparator dedicated to a single instruction in the bundle;  
5 wherein  
each RD field of the in-flight instructions is compared by a single entry  
structure to all instructions in the bundle substantially simultaneously.
25. The computer system of Claim 24 wherein the hit detect signal further  
comprises an array of the second predetermined number by the third  
predetermined number in size, which includes the output of hits detected for  
each of the entry structures compared to each of the instructions in the bundle.  
5
26. A method for performing out of order processing on an instruction set  
having a plurality of instructions with a superscalar processor, the method  
comprising:  
fetching the instructions from the instruction set;  
5 renaming architectural registers associated with the instructions to  
physical registers during the processing of the instruction set;  
transmitting a first output signal from a content addressable memory  
(CAM) structure for generating dependency data of in-flight instructions of the  
instruction set;  
10 transmitting a second output signal from the CAM structure for  
generating physical register address data necessary to execute the in-flight  
instructions when the dependency data indicates that the dependencies of the  
in-flight instructions have been removed;  
storing the dependency data in a dependency matrix;  
15 storing the physical register address data in an instruction wait buffer;  
scheduling the in-flight instructions for execution based on the  
dependency data and the physical register address data; and  
executing the in-flight instructions.

27. The method of Claim 26 wherein transmitting the first output signal further comprises:

transmitting a plurality of first output signals from a plurality of CAM structures; and

5 logically OR-ing the first output signals to generate the dependency data.

28. The method of Claim 26 wherein the instructions have a first predetermined maximum number of register source fields (RS fields) having architectural addresses for instruction input data and at least a maximum  
10 number of one register destination fields (RD fields) having architectural addresses for instruction output data, and wherein the transmitting the first output signal further comprises:

comparing an RS field of a fetched instruction to an RD field of an in-flight instruction within a comparator section of the CAM structure; and

15 generating a hit detect signal indicative of the architectural address of the RD field when the RS field and the RD field match, i.e., hit; and

transmitting the hit detect signal additionally to an array section of the CAM structure.

29. The method of Claim 28 wherein transmitting the second output signal further comprises generating the second output signal when the array section receives the hit detect signal, the second output signal being indicative of the physical register address of the RD field.

30. The method of Claim 29 wherein the CAM structure further comprises a plurality of the first predetermined number of CAM structures, each CAM structure being dedicated to a single RS field.

31. The method of Claim 30 further comprising logically OR-ing the hit detect signals of each CAM structure to generate the dependency data.

32. The method of Claim 31 further comprising:  
 fetching a bundle of instructions from the instruction set;  
 generating an intra-dependency signal indicative of intra-dependencies of  
 instructions within the bundle;
- 5 combining the intra-dependency signal with the OR-ed output signals of  
 the hit detect signals to generate the dependency data.

10  
15  
20  
25  
30  
35  
40  
45  
50  
55  
60  
65  
70  
75  
80  
85  
90  
95  
100  
105  
110  
115  
120  
125  
130  
135  
140  
145  
150  
155  
160  
165  
170  
175  
180  
185  
190  
195  
200  
205  
210  
215  
220  
225  
230  
235  
240  
245  
250  
255  
260  
265  
270  
275  
280  
285  
290  
295  
300  
305  
310  
315  
320  
325  
330  
335  
340  
345  
350  
355  
360  
365  
370  
375  
380  
385  
390  
395  
400  
405  
410  
415  
420  
425  
430  
435  
440  
445  
450  
455  
460  
465  
470  
475  
480  
485  
490  
495  
500  
505  
510  
515  
520  
525  
530  
535  
540  
545  
550  
555  
560  
565  
570  
575  
580  
585  
590  
595  
600  
605  
610  
615  
620  
625  
630  
635  
640  
645  
650  
655  
660  
665  
670  
675  
680  
685  
690  
695  
700  
705  
710  
715  
720  
725  
730  
735  
740  
745  
750  
755  
760  
765  
770  
775  
780  
785  
790  
795  
800  
805  
810  
815  
820  
825  
830  
835  
840  
845  
850  
855  
860  
865  
870  
875  
880  
885  
890  
895  
900  
905  
910  
915  
920  
925  
930  
935  
940  
945  
950  
955  
960  
965  
970  
975  
980  
985  
990  
995